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XILINX, INC ATTN: LEGAL DEPARTMENT 2100 LOGIC DR SAN JOSE, CA 95124				WILLIAMS, ALEXANDER O
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DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/698,704	CONN, ROBERT O.
	Examiner Alexander O. Williams	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 29 June 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8 and 12-16 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-8 and 12-16 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 10/31/03 & 8/30/04.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

Serial Number: 10/698704 Attorney's Docket #: X-1416-3US
Filing Date: 10/31/2003;

Applicant: Conn

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 8 and 12 to 16) filed 6/29/05 to the species elected of species of figures 1 to 7 filed 4/4/05 has been acknowledged.

Claims 9-11 have been cancelled.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim 2 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, it is unclear and confusing to what is meant by "wherein a line extending through the first micro-bump in a direction orthogonal to the surface of the integrated circuit **does not extend through the first landing pad of the integrated circuit package.**"

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

Claims 1 to 8 and 12 to 16, **insofar as claim 2 can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Yamagishi et al. (U.S. Patent Application Publication # 2004/0239349 A1).

1. Yamagishi et al. (figures 1 to 16) specifically figure 1A show an assembly, comprising: an integrated circuit die 101 having an array of micro-bumps 103A disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 104 having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure 102 disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed in a different position in the array of landing pads.

2. The assembly of claim 1, Yamagishi et al. show wherein a line extending through the first micro-bump in a direction orthogonal to the surface of the integrated circuit does not extend through the first landing pad of the integrated circuit package.
3. The assembly of claim 2, Yamagishi et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the interposing structure have roughly identical surface areas.
4. The assembly of claim 3, Yamagishi et al. show wherein the interposing structure includes no transistor and no PN junction.
5. The assembly of claim 4, Yamagishi et al. show wherein the interposing structure comprises an array of micro-bumps, wherein the array of micro-bumps of the interposing structure has a pattern that is substantially identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.
6. The assembly of claim 5, Yamagishi et al. show wherein the interposing structure includes a layer comprising epoxy and fiberglass.
7. The assembly of claim 5, Yamagishi et al. show wherein the interposing structure includes a bypass capacitor.
8. The assembly of claim 5, Yamagishi et al. show wherein the first micro-bump is coupled to the first landing pad at least in part by a conductor disposed in the interposing structure, wherein the conductor disposed in the interposing structure extends in a direction parallel to the surface of the integrated circuit.
12. Yamagishi et al. (figures 1 to 16) specifically figure 1A show an assembly **100**, comprising: an integrated circuit die **101** having an array of micro-bumps **103A** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **104** having an array of landing pads disposed on an inside surface of the integrated circuit package in a

second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and means **102** for coupling a first micro-bump in a first position in the array of microbumps to a first landing pad disposed in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

13. The assembly of claim 12, Yamagishi et al. show wherein the means is also for providing a bypass current to the integrated circuit die.

14. The assembly of claim 12, Yamagishi et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the means has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the means have roughly identical surface areas.

15. The assembly of claim 12, Yamagishi et al. show wherein the means has a planar form and is less than 500 microns thick.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

16. The assembly of claim 12, Yamagishi et al. show wherein the integrated circuit die is an application specific integrated circuit (ASIC) (inherent).

A decoupling capacitor (or bypass capacitor) is commonly used with the semiconductor integrated circuit (IC) chip to reduce the noise in the power supplied to the IC chip. Advances in IC technology have increased the switching speeds employed by the recent IC devices, so that many IC chips are capable of operation at high frequencies, or microwave frequencies. High switching speeds increase the problem of power supply noise, a component of which is generated as the device is switched on and off. In order for the IC chip to function properly, the power supplied must be free from noise.

[0005] Japanese Laid-Open Patent Application 7-111280 discloses another probe card that carries a plurality of probes at a rear surface of the probe card. In this construction, the

interconnection pattern is provided on the front surface, and various exterior circuit parts such as bypass capacitors or wave-shaping circuits are connected to this interconnection pattern at the front side of the probe card substrate. Such a construction of providing the probes and exotic circuit components at different sides of the probe card substrate makes it possible to dispose the exotic circuit components immediately adjacent to the probes. Thereby, the accuracy of testing is improved.

[0020] FIGS. 1A and 1B show the construction of a semiconductor device 100 having an interposer-type decoupling capacitor.

[0021] Referring to FIG. 1A, the semiconductor device 100 has a construction in which an interposer-type decoupling capacitor 102 is mounted upon a semiconductor chip by way of bumps 103A. Further, the decoupling capacitor 102 thus carrying the semiconductor chip 101 thereon is mounted on a package substrate 104 by way of bumps 103B. Further, the package substrate 104 thus carrying thereon the decoupling capacitor 102 and the semiconductor chip 101 is mounted on a circuit substrate 105 by way of bumps 106.

Claims 1 to 8 and 12 to 16, **insofar as claim 2 can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Moro et al. (U.S. Patent Application Publication # 2002/0088977 A1).

1. Mori et al. (figures 1A to 18) specifically figure 11 show an assembly, comprising: an integrated circuit die 57 having an array of micro-bumps 58 disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 64 having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure 62 disposed inside the integrated

circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed in a different position in the array of landing pads.

2. The assembly of claim 1, Mori et al. show wherein a line extending through the first micro-bump in a direction orthogonal to the surface of the integrated circuit does not extend through the first landing pad of the integrated circuit package.
3. The assembly of claim 2, Mori et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the interposing structure have roughly identical surface areas.
4. The assembly of claim 3, Mori et al. show wherein the interposing structure includes no transistor and no PN junction.
5. The assembly of claim 4, Mori et al. show wherein the interposing structure comprises an array of micro-bumps, wherein the array of micro-bumps of the interposing structure has a pattern that is substantially identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.
6. The assembly of claim 5, Mori et al. show wherein the interposing structure includes a layer comprising epoxy and fiberglass.
7. The assembly of claim 5, Mori et al. show wherein the interposing structure includes a bypass capacitor (decoupling capacitor).
8. The assembly of claim 5, Mori et al. show wherein the first micro-bump is coupled to the first landing pad at least in part by a conductor disposed in the interposing structure, wherein the conductor disposed in the interposing

structure extends in a direction parallel to the surface of the integrated circuit.

12. Mori et al. (figures 1A to 18) specifically figure 11 show an assembly, comprising: an integrated circuit die 57 having an array of micro-bumps 58 disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 64 having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and means 62 for coupling a first micro-bump in a first position in the array of microbumps to a first landing pad disposed in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

13. The assembly of claim 12, Mori et al. show wherein the means is also for providing a bypass current to the integrated circuit die (decoupling capacitor).

14. The assembly of claim 12, Mori et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the means has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the means have roughly identical surface areas.

15. The assembly of claim 12, Mori et al. show wherein the means has a planar form and is less than 500 microns thick.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

16. The assembly of claim 12, Mori et al. show wherein the integrated circuit die is an application specific integrated circuit (ASIC) (inherent).

[0025] It is a still further object of the present invention to provide a novel stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale

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integrated circuit, and the stacked capacitor has a high capacity for a unit packaging area.

[0027] It is further more object of the present invention to provide a novel stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale integrated circuit, and the stacked capacitor allows a reduction of a total inductance of the capacitor and a wiring.

[0028] It is more over object of the present invention to provide a novel stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor reduces a signal transmission delay.

[0031] It is another object of the present invention to provide a novel method of forming a stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale integrated circuit, and the stacked capacitor has a high capacity for a unit packaging area.

[0033] It is further another object of the present invention to provide a novel method of forming a stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale integrated circuit, and the stacked capacitor allows a reduction of a total inductance of the capacitor and a wiring.

[0034] It is furthermore another object of the present invention to provide a novel method of forming a stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor reduces a signal transmission delay.

[0037] It is an additional object of the present invention to provide a novel semiconductor device including a stacked

capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale integrated circuit, and the stacked capacitor has a high capacity for a unit packaging area.

TWELFTH EMBODIMENT

[0119] A twelfth embodiment according to the present invention will be described with reference to the drawings. FIG. 11 is a cross sectional elevation view of a semiconductor device over a circuit board in a twelfth embodiment according to the present invention. A stacked capacitor 62 is provided as an interposer between a printed circuit board 64 and a large scale integrated circuit bare chip 57. The stacked capacitor 62 is electrically connected to the large scale integrated circuit bare chip 57 through first, second and third terminal electrodes 59, 60, and 61 and solder bumps 58. The stacked capacitor 62 is also electrically connected to the printed circuit board 64 through the first, second and third terminal electrodes 59, 60, and 61 and the solder bumps 58. The first terminal electrode 59 is connected to the signal line of the large scale integrated circuit. The second terminal electrode 60 is connected to the power line. The third terminal electrode 61 is connected to the ground line.

Claims 1 to 8 and 12 to 16, **insofar as claim 2 can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Winer et al. (U.S. Patent # 6,525,922 B2).

1. Winer et al. (figures 1 to 13) specifically figures 1 show an assembly 10, comprising: an integrated circuit die 12 having an array of micro-bumps 20 disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 16 having an array of landing pads (inherent) disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure 14 disposed inside the integrated

circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed in a different position in the array of landing pads.

2. The assembly of claim 1, Winer et al. show wherein a line extending through the first micro-bump in a direction orthogonal to the surface of the integrated circuit does not extend through the first landing pad of the integrated circuit package.
3. The assembly of claim 2, Winer et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the interposing structure have roughly identical surface areas.
4. The assembly of claim 3, Winer et al. show wherein the interposing structure includes no transistor and no PN junction.
5. The assembly of claim 4, Winer et al. show wherein the interposing structure comprises an array of micro-bumps, wherein the array of micro-bumps of the interposing structure has a pattern that is substantially identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.
6. The assembly of claim 5, Winer et al. show wherein the interposing structure includes a layer comprising epoxy and fiberglass.
7. The assembly of claim 5, Winer et al. show wherein the interposing structure includes a bypass capacitor (de-coupling capacitor).
8. The assembly of claim 5, Winer et al. show wherein the first micro-bump is coupled to the first landing pad at least in part by a conductor disposed in the interposing structure, wherein the conductor

disposed in the interposing structure extends in a direction parallel to the surface of the integrated circuit.

12. Winer et al. (figures 1 to 13) specifically figures 1 show an assembly, comprising: an integrated circuit die **12** having an array of micro-bumps **20** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **16** having an array of landing pads (inherent) disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and means **14** for coupling a first micro-bump in a first position in the array of microbumps to a first landing pad disposed in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

13. The assembly of claim 12, Winer et al. show wherein the means is also for providing a bypass current to the integrated circuit die (de-coupling capacitor).

14. The assembly of claim 12, Winer et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the means has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the means have roughly identical surface areas.

15. The assembly of claim 12, Winer et al. show wherein the means has a planar form and is less than 500 microns thick.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

16. The assembly of claim 12, Winer et al. show wherein the integrated circuit die is an application specific integrated circuit (ASIC) (inherent).

[0010] As shown in FIG. 1, the microprocessor assembly 10 uses flip chip technology to interconnect the various components. Flip chip technology is an interconnection scheme that allows a number of contact terminals on a first structure to be simultaneously coupled to corresponding terminals on a second

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structure. Bumps of solder (or another metal alloy) are first deposited on the contact pads of the first structure. These solder bumps are then aligned with corresponding contact pads on the second structure. After alignment, the solder bumps are conductively bonded to the contact pads of the second structure using, for example, solder reflow or ultrasonic bonding. With reference to FIG. 1, solder bumps 18 on the underside of the interposer unit 14 are aligned with and bonded to contact pads on the package substrate 16, as described above. Contact pads on the underside of the die 12 are then aligned with and bonded to solder bumps 20 on the top of the interposer unit 14 in a similar manner. It should be appreciated that the solder bumps 18, 20 could alternatively (or in addition) have been placed on the package substrate 16 and the die 12, respectively, before alignment. Typically, the contact pattern on the top of the interposer unit 14 will be the same as the pattern on the surface of the package substrate 16 (although in at least one embodiment a different pattern is used). The number and arrangement of the contacts on the underside of the die 12 will typically be specific to the particular implementation. As shown in FIG. 1, an optional composite underfill material 22 (e.g., epoxy) can be provided to fill the gaps between the bumps 18, 20 to provide rigidity and structural integrity to the assembly 10. It should be appreciated that other methods or combinations of methods for providing interconnection between the die 12, the interposer unit 14, and the package substrate 16 can alternatively be used, as will be apparent to a person of ordinary skill in the art.

[0011] FIG. 2 is a sectional side view of a portion of the interposer unit 14 of FIG. 1 in one embodiment of the present invention. As illustrated, the interposer unit 14 includes a plurality of solder bumps 18 on a lower surface thereof to provide electrical connection to the package substrate 16 and a plurality of solder bumps 20 on an upper surface thereof to provide electrical connection to the die 12. In addition, each of the solder bumps 20 on the upper surface of the interposer unit 14 has a corresponding solder bump 18 on the bottom surface of the unit 14. The interposer unit 14 includes a conductive connection between each of these solder bump "pairs" to conductively couple a contact pad on the die 12 to a corresponding contact pad on the package substrate 16. In the illustrated embodiment, for example, one of the solder bump pairs of the interposer unit 14 corresponds to a first supply

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terminal V.sub.CC that is to be coupled to the die 12. Another solder bump pair corresponds to a second supply terminal V.sub.SS that is to be coupled to the die 12. Thus, the V.sub.CC contact pad on the package substrate 16 will be directly connected to the V.sub.CC terminal on the die 12 and the V.sub.SS contact pad on the package substrate 16 will be directly connected to the V.sub.SS terminal on the die 12 through the interposer unit 14 to provide power to the die 12 during circuit operation. Similarly, a plurality of other solder bump pairs will typically exist that each correspond to one of the input/output connections between the die 12 and the package substrate 16. These pairs will also be directly connected through the interposer unit 14. In addition to the through connections described above, the interposer unit 14 also provides a decoupling capacitance between the V.sub.CC terminal and the V.sub.SS terminal of the die 12.

[0012] With reference to FIG. 2, the interposer unit 14 is formed from a single substrate member 30 having a plurality of via holes 32 extending there through. In a preferred approach, the substrate member 30 consists of a semiconductor material (such as, for example, silicon or germanium), although other substrate materials can alternatively be used. As illustrated, the interposer unit 14 is formed by building up various material layers on the substrate member 30 both inside and outside the via holes 32. A first metallization layer 34 forms an inner metallic member of the interposer unit 14. The first metallization layer 34 is covered with an insulating layer 36 which, in turn, is covered with a second metallization layer 38. The solder bumps 18, 20 corresponding to the V.sub.CC terminal are conductively coupled to the second metallization layer 38 which provides the V.sub.CC connection through the interposer unit 14. Similarly, the solder bumps 18, 20 corresponding to the V.sub.SS terminal are conductively coupled to the first metallization layer 34 which provides the V.sub.SS connection through the interposer unit 14. In addition, the relatively thin insulating layer 36 between the first and second metallization layers 34, 38 causes a relatively large capacitance to be formed between the first and second metallization layers 34, 38 and thus between the supply terminals V.sub.CC and V.sub.SS. Because the via holes 32 are used, the effective surface area of the capacitor plates is relatively large for the size of the interposer unit 14, thus resulting in a relatively large de-coupling capacitance within the interposer unit 14. Also, as the number of via holes 32

that are used to form the capacitor is increased, the series resistance and inductance of the capacitor will correspondingly decrease as the incremental inductance and capacitance associated with each via is added in parallel. This decrease in series inductance and resistance is beneficial for circuits (e.g., microprocessor circuits) that may require quick changes in current (i.e., high di/dt) to compensate for such things as voltage droop and the like.

[0013] In the illustrated embodiment, a portion of the first metallization layer 34 acts as the first plate of the de-coupling capacitor and a portion of the second metallization layer 38 acts as the second plate of the de-coupling capacitor. In the region of the I/O connection, however, other portions of the first and second metallization layers 34, 38 are isolated from the portions providing the de-coupling capacitance and thus do not contribute to the total capacitance. This is because the I/O connections do not generally require a shunt capacitance. With reference to FIG. 2, the solder bumps 18, 20 corresponding to the I/O terminal are each coupled to the first metallization layer 38 to provide the conductive I/O connection through the interposer unit 14 (i.e., through the corresponding via hole 32). However, channels 40 have been etched through the first and second metallization layers 34, 38 in the region about the I/O connection to isolate the layers 34, 38 as described above. Thus, the I/O connection through the interposer unit 14 is not coupled to either plate of the de-coupling capacitor. A similar isolation technique is preferably used for each of the other I/O connections through the interposer unit 14.

[0022] As described above in connection with FIG. 1, a variety of different techniques can be used in accordance with the present invention to interconnect the die 12, the interposer unit 14, and the package substrate 16. For example, mounting techniques such as tape-automated bonding (TAB) or wire bonding can be used. In addition, combinations of different technologies can be implemented. In one embodiment, for example, flip chip techniques are used on one side of the interposer unit 14 and wire bonding is used on the other side. More complex combinations are also possible. For example, in one implementation, the die is mounted into an inverted cavity pin grid array package using wire bonding at the periphery of the die. The via capacitor is then mounted to the die using solder bumps in the center. Many other techniques and combinations of techniques can also be used.

[0023] It should be appreciated that the inventive principles are not limited to implementation within an interposer unit as described above. For example, in one embodiment of the invention, a via capacitor is implemented within an integrated circuit package (e.g., as part of the package substrate) to provide de-coupling for a corresponding die. In another embodiment, a via capacitor is implemented on the die itself. In yet another embodiment, a separate via capacitor is bonded to the die in a location that is not between the die and the package substrate. As will be apparent to persons of ordinary skill in the art, other configurations are also possible. The via capacitor can be smaller, larger, or the same size as the die. In one approach, a via capacitor is fabricated using a silicon/insulator/metal stack. In another approach, a via capacitor is fabricated using multiple or repeating metal/oxide stacks. It should also be appreciated that the inventive principles are not limited to use in providing **de-coupling functions**. On the contrary, the inventive principles can be implemented in any of a wide variety of different integrated circuit applications that require high performance capacitors. Furthermore, it should be understood that embodiments of the invention exist where the via holes do not extend fully through the substrate.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a plurality of chips and a chip deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of

obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1 to 8 and 12 to 16, **insofar as claim 2 can be understood**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Berlin et al. (U.S. Patent # 6,104,082).

1. Berlin et al. (figures 1 to 13b) specifically figure 2b discloses an assembly, comprising: an integrated circuit die (chips 1-6) having an array of micro-bumps 62 disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 68 having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure 60' disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed in a different position in the array of landing pads.
2. The assembly of claim 1, Berlin et al. show wherein a line extending through the first micro-bump in a direction orthogonal to

the surface of the integrated circuit does not extend through the first landing pad of the integrated circuit package.

3. The assembly of claim 2, Berlin et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the interposing structure have roughly identical surface areas.

4. The assembly of claim 3, Berlin et al. show wherein the interposing structure includes no transistor and no PN junction.

5. The assembly of claim 4, Berlin et al. show wherein the interposing structure comprises an array of micro-bumps, wherein the array of micro-bumps of the interposing structure has a pattern that is substantially identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.

6. The assembly of claim 5, Berlin et al. show wherein the interposing structure includes a layer comprising epoxy and fiberglass.

7. The assembly of claim 5, Berlin et al. show wherein the interposing structure includes a bypass capacitor.

8. The assembly of claim 5, Berlin et al. show wherein the first micro-bump is coupled to the first landing pad at least in part by a conductor disposed in the interposing structure, wherein the conductor disposed in the interposing structure extends in a direction parallel to the surface of the integrated circuit.

12. Berlin et al. (figures 1 to 13b) specifically figure 2b discloses an assembly, comprising: an integrated circuit die (**chips 1-6**) having an array of micro-bumps **62** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **68** having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and means **60'** for coupling a first micro-bump in a first

position in the array of microbumps to a first landing pad disposed in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

13. The assembly of claim 12, Berlin et al. show wherein the means is also for providing a bypass current to the integrated circuit die.

14. The assembly of claim 12, Berlin et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the means has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the means have roughly identical surface areas.

15. The assembly of claim 12, Berlin et al. show wherein the means has a planar form and is less than 500 microns thick.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

16. The assembly of claim 12, Berlin et al. show wherein the integrated circuit die is an application specific integrated circuit (ASIC).

As shown in FIG. 2b, pad extensions 46, 48 are connected through bump connectors 62 to pads 64 on interposer 60'. Each bump connector 62 contacting interposer 60' can be located in either of two positions 64a, 64b on pad 64 to enable contact of pad 64 to either of two adjacent chips. Thus, bump connector 62a located in position 64a contacts chip 1 rather than chip 2 whereas bump connector 62b located in position 64b contacts chip 3 rather than chip 2. Straight connections through interposer 60' to substrate-connect pads 66 can now be provided, the winding path of metallization 50 through open and closed fuses 52 of FIGS. 1d and 2a being no longer needed.

(9) Using the placement of bump 62 as a selection means, it is possible to bypass connection to a chip pad. Accordingly, FIG. 1c' may be used instead of FIG. 1c, with face 32' not requiring fuse 44, 44' shown in FIG. 1c.

(10) Interposer 60' is itself connected to substrate 68 through bump connectors 69. Bump connectors 62 and 69 are formed using

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connector techniques, such as C4 solder bumps, solder paste, conductive paste, or gold bumps, all well known in the art. Gold bumps are most conveniently provided on interposer pad 64 using conventional gold bump technology in which a wire bonder is programmed to locate the gold bump where desired based on chip pass-fail data. Conductive paste is advantageous since it is reworkable. A bump encapsulant material such as a high temperature filled epoxy (for example, Dexter Hysol 4526 encapsulant or Locktite 3510) is used under interposer to reduce stress from thermal expansion mismatch. A ground plane, or a power plane, or a split ground and power plane, or separate ground and power planes may be included in interposer 60' for enhanced electrical performance (e.g., reduced inductance, decoupling capacitor options, etc.).

(11) In addition to bump placement variation, selective connection between metallization on interposer 60 and level 40 on side face 32 of stack 16 can also be accomplished using flex-type interposer 60" having ribbon bonds 70, as shown in FIG. 2c. Ribbon bonds 70 accomplish the function of the metallization level 50 and fuses 52 of FIGS. 1c, 2a or of the variable location bump connectors 62 of FIG. 2b, by selectively making connection where needed. By contrast, in FIG. 2a, connection was selectively deleted with fuses and in FIG. 2b connection was provided by selectively locating the entire bump connector. Interposer 60" of FIG. 2c has ribbon bond 70 supported on tape 72 having adhesive 74 for secure fastening to side face 32. In this embodiment, ribbon bonds 70 eliminate the need either for fuses (FIG. 2a) or selective bumps (FIG. 2b). Thermal expansion mismatch stress between side face 32 and interposer 60" is accommodated through the use of a low modulus, silicon-based adhesive (e.g., Dow Corning 7910 Chip Scale Encapsulant). The interposer 60" is selected to have a coefficient thermal expansion (CTE) similar to that of the next level of assembly (e.g., CTE in the range of 10-20 ppm/.degree. C.) while the chip has a CTE of approximately 3 ppm/.degree. C. Additionally, the ribbon bonds provide a highly reliable, compliant electrical interconnection between side face 32 and interposer 60" for enhanced electrical performance (e.g., reduced inductance, decoupling capacitor options, etc.).

(32) The tailorabile metallization of the present invention also provides a scheme for rapidly creating or altering circuit configurations; in essence application specific integrated

circuits are quickly fabricated by selecting and deselecting circuits with the metallization tailoring methods disclosed herein. While it would be advantageous to test circuit elements first to ensure the functionality of the included circuits before finalizing the metallization, these ASIC circuits could also be built with the tailorabile wiring of the present invention without the intermediate test. The wiring can be tailored by methods such as opening fuses, providing ribbon connections, providing bump connections, or providing photolithographically formed shapes as described herein above.. In this case, defective circuits would be included and would result in yield loss but other functional chips would be fabricated in much less time than would be required to provide masks.

Therefore, it would have been obvious to one of ordinary skill in the art to use the plurality of chips and the chip as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamagishi et al. (U.S. Patent Application Publication # 2004/0239349 A1) in view of Berlin et al. (U.S. Patent # 6,104,082).

Yamagishi et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the integrated circuit die is an application specific integrated circuit (ASIC).

Berlin et al. show a metallization structure for altering connections. Specifically, Berlin et al. (figures 1 to 13b) specifically figure 2b discloses an assembly, comprising: an integrated circuit die (chips 1-6) having an array of micro-bumps 62 disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 68 having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure 60' disposed inside the integrated circuit package between the integrated circuit die and the inside surface of

the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed in a different position in the array of landing pads, wherein the integrated circuit die (**chips 1-6**) is an application specific integrated circuit (ASIC) for the purpose of providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

(32) The tailorable metallization of the present invention also provides a scheme for rapidly creating or altering circuit configurations; in essence application specific integrated circuits are quickly fabricated by selecting and deselecting circuits with the metallization tailoring methods disclosed herein. While it would be advantageous to test circuit elements first to ensure the functionality of the included circuits before finalizing the metallization, these ASIC circuits could also be built with the tailorable wiring of the present invention without the intermediate test. The wiring can be tailored by methods such as opening fuses, providing ribbon connections, providing bump connections, or providing photolithographically formed shapes as described herein above. In this case, defective circuits would be included and would result in yield loss but other functional chips would be fabricated in much less time than would be required to provide masks.

Therefore, it would have been obvious to one of ordinary skill in the art to use Berlin et al.'s ASIC chip type to modify Yamagishi et al.'s chip for the purpose of providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

Claims 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Winer et al. (U.S. Patent # 6,525,922 B2) in view of Berlin et al. (U.S. Patent # 6,104,082).

Winer et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the integrated circuit die is an application specific integrated circuit (ASIC).

Berlin et al. show a metallization structure for altering connections. Specifically, Berlin et al. (figures 1 to 13b) specifically figure 2b discloses an assembly,

comprising: an integrated circuit die (chips 1-6) having an array of micro-bumps 62 disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 68 having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure 60' disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed in a different position in the array of landing pads, wherein the integrated circuit die (**chips 1-6**) is an application specific integrated circuit (ASIC) for the purpose of providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

(32) The tailorable metallization of the present invention also provides a scheme for rapidly creating or altering circuit configurations; in essence application specific integrated circuits are quickly fabricated by selecting and deselecting circuits with the metallization tailoring methods disclosed herein. While it would be advantageous to test circuit elements first to ensure the functionality of the included circuits before finalizing the metallization, these ASIC circuits could also be built with the tailorable wiring of the present invention without the intermediate test. The wiring can be tailored by methods such as opening fuses, providing ribbon connections, providing bump connections, or providing photolithographically formed shapes as described herein above. In this case, defective circuits would be included and would result in yield loss but other functional chips would be fabricated in much less time than would be required to provide masks.

Therefore, it would have been obvious to one of ordinary skill in the art to use Berlin et al.'s ASIC chip type to modify Winer et al.'s chip for the purpose of

providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

Claims 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Moro et al. (U.S. Patent Application Publication # 2002/0088977 A1) in view of Berlin et al. (U.S. Patent # 6,104,082).

Moro et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the integrated circuit die is an application specific integrated circuit (ASIC).

Berlin et al. show a metallization structure for altering connections. Specifically, Berlin et al. (figures 1 to 13b) specifically figure 2b discloses an assembly, comprising: an integrated circuit die (chips 1-6) having an array of micro-bumps 62 disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 68 having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure 60' disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed in a different position in the array of landing pads, wherein the integrated circuit die (**chips 1-6**) is an application specific integrated circuit (ASIC) for the purpose of providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

(32) The tailorabile metallization of the present invention also provides a scheme for rapidly creating or altering circuit configurations; in essence application specific integrated circuits are quickly fabricated by selecting and deselecting circuits with the metallization tailoring methods disclosed

herein. While it would be advantageous to test circuit elements first to ensure the functionality of the included circuits before finalizing the metallization, these ASIC circuits could also be built with the tailorabile wiring of the present invention without the intermediate test. The wiring can be tailored by methods such as opening fuses, providing ribbon connections, providing bump connections, or providing photolithographically formed shapes as described herein above. In this case, defective circuits would be included and would result in yield loss but other functional chips would be fabricated in much less time than would be required to provide masks.

Therefore, it would have been obvious to one of ordinary skill in the art to use Berlin et al.'s ASIC chip type to modify Moro et al.'s chip for the purpose of providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/653,758,774,778,737,738,734,686,685,723,691,774,6 92,693 361/306.3,312,313,321.1,321.4	9/11/05
Other Documentation: foreign patents and literature in 257/653,758,774,778,737,738,734,686,685,723,691,774,6 92,693 361/306.3,312,313,321.1,321.4	9/11/05
Electronic data base(s): U.S. Patents EAST	9/11/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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